

Transient Thermal Compact Models for Circuit Simulation

Adam Augustin and Torsten Hauck

Freescale Semiconductor, Schatzbogen 7, D-81829 Munich, Germany
adam.augustin@freescale.com, torsten.hauck@freescale.com

Abstract—The paper presents a boundary condition independent transient thermal network model generated by means of model order reduction methods. The order reduction is performed with *MOR for ANSYS* which is based on the Krylov subspace method via the Arnoldi algorithm. Subsystems such as a semiconductor device and the printed circuit board are modeled with ANSYS, separately. Then, these models are used for the network generation.

By means of model coupling thermal system simulation is presented. Simulation results of the coupled sub models are compared with ANSYS simulations of the full model.

I. INTRODUCTION

For complex package and heat source configurations as well as for different applications, accurate thermal models are needed. Several thermal modeling techniques are available beginning with analytical approaches [1], [2] for simple geometrical structures and ending with numerical finite element (FE) methods, which are implemented in powerful simulators such as ANSYS® [3]. This numerical approach allows the covering of very complex geometrical problems without any remarkable limitations.

Because of the high packing density in semiconductor devices thermal modeling becomes here more and more challenging. The number of heat sources continuously increase causing a large number of degrees of freedom (DOFs) in the FE-model. This matter of fact together with complex loading profiles increase the necessary simulation time which is undesirable within the product development process.

To overcome these circumstances modern mathematical approaches can be used to reduce the order of models [4]. Taking a high dimensional finite element model a formal model reduction approach [5] allows the generation of its low-dimensional approximation. Several research groups have already documented its successful application to thermal problems [6], [7]. Even semiconductor devices with multiple heat sources can be treated very well as have been shown in [8].

Another excessively covered topic is the generation of compact thermal models [9]–[12]. Compact models reduces the simulation time dramatically and by conjoining them with electrical network models a coupled electro-thermal simulation becomes possible. Using reduced models in state space representation compact network models can be generated [13]–[16]. The presented networks are usually realized as small subnetworks with controlled

components such as voltage-dependent current sources and vice versa. Our network model is represented by the capacitance and conductance matrix what is a more “natural” network representation.

The paper is structured as follows. In the next section we will introduce our new boundary condition independent compact model describing the components as sub models. Additionally, a convection model for non-homogeneous distributed temperature on surface will be presented here as well. Section III shows the implementation of the models into a network simulator. In section IV an application is described following by comparative results in section V. Finally, some conclusions follow in section VI.

II. NETWORK MODEL

For a system simulation by means of model coupling, sub models representing particular components should be modeled by boundary condition independent Kirchhoffian networks. In these models, flow and potential is defined on each port, as well as the Kirchhoff current laws are satisfied on all nodes. This makes it possible to couple the models at their appropriate ports, arbitrarily.

A. Kirchhoff Network Representation

A necessary condition for the generation of Kirchhoffian network models is the identical number n of inputs and outputs in the state space model. Additionally, since in a Kirchhoffian network on each IO-port (input-output-port) a well defined current and potential is given, all nodes of the area representing a port in the FE-model must be constraint by the command `CP, NEXT, TEMP, ALL`. This procedure reduces the DOF `TEMP` of all selected nodes to the node with the lowest number. Fig. 1 shows the symbols used by ANSYS indicating the executed command. The top left

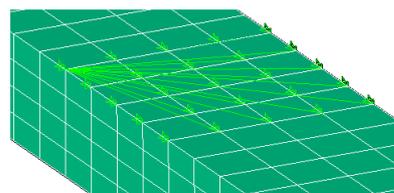


Fig. 1. Command `CP, NEXT, TEMP, ALL` applied on some selected nodes in order to confine the DOF'S to the temperature of the node with lowest number

node has the lowest number. These two constraints guarantee, that after several matrix manipulations we obtain on every IO-port of the Kirchoffian network a well defined current and potential.

To keep the network size practicable we use model order reduction methods which provide very small models with a negligible loss of accuracy [8], [17]. For the reduction process we use the software *MOR for ANSYS* [18] developed on IMTEK, University of Freiburg. It is an open source command-line tool built on top of the ANSYS-supplied library to read ANSYS binary files. The information from ANSYS models is read from *.full and *.emat files. *MOR for ANSYS* generates reduced models in state space representation by means of Krylov subspaces which are built via the block Arnoldi algorithm [19].

The reduced model with order m in state space representation is expressed as

$$\begin{aligned} M \dot{z}(t) + A z(t) &= B_e u(t) \\ y(t) &= C_e z(t) \end{aligned} \quad (1)$$

where $y(t)$ is the $n \times 1$ output vector of unknown temperatures, $u(t)$ is the $n \times 1$ input vector and $z(t)$ is the $m \times 1$ state vector of the reduced model. For the dimensions we assume arbitrarily that $m > n$. The dimensions of the four matrices are: output matrix $C_e^{n \times m}$, input matrix $B_e^{m \times n}$, capacity matrix $M^{m \times m}$ and conductivity matrix $A^{m \times m}$. Index e indicates here the matrices representing external ports.

In order to transform eq. (1) into a network representation the matrices B_e and C_e must be expanded to quadratic matrices

$$B^{m \times m} = \begin{bmatrix} B_e & B_i \end{bmatrix} \quad \text{and} \quad C^{m \times m} = \begin{bmatrix} C_e \\ C_i \end{bmatrix} \quad (2)$$

with B_i and C_i indicating the internal nodes. With the potential vector $T(t)$ and the electrical flow vector $P(t)$ the Kirchoffian network representation of eq. (1) can be written as

$$H \dot{T}(t) + K T(t) = P(t) \quad (3)$$

with the capacitance matrix $H = B^{-1} M C^{-1}$ and the conductance matrix $K = B^{-1} A C^{-1}$.

B. Convection Model Dealing with Hot Spots

Generally, on surfaces with convection as boundary condition the temperature distribution is not homogeneous distributed over the entire surface. For a port describing a surface with the method shown in section II-A, where a surface load is constrained to the node with the lowest number, we obtain only one value for the temperature of the entire surface. To overcome this disadvantage the surface must be described by a set of ports. This is possible by using Lagrange polynomials describing the heat flux as function of the surface coordinates. In doing so, the number of ports depends on the order of the Lagrange

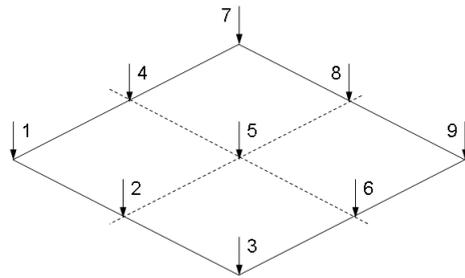


Fig. 2. Surface with ports for convection definition with Lagrange polynomials of order two. The arrows indicate the flux the non homogeneous surface temperature with Lagrange polynomial of order two

polynomial. For instance, Fig. 2 shows the distribution of nine ports for Lagrange polynomials of order two. Using at least this order, the description of one hot spot on the surface will be possible.

Since in ANSYS it is not possible to apply heat flux on elements (SFE, HFLUX) using different values for each node associated to this element, the flux must be recalculated. In doing so, by means of the command F, HEAT, different values on each node can be applied. Fig. 3 shows

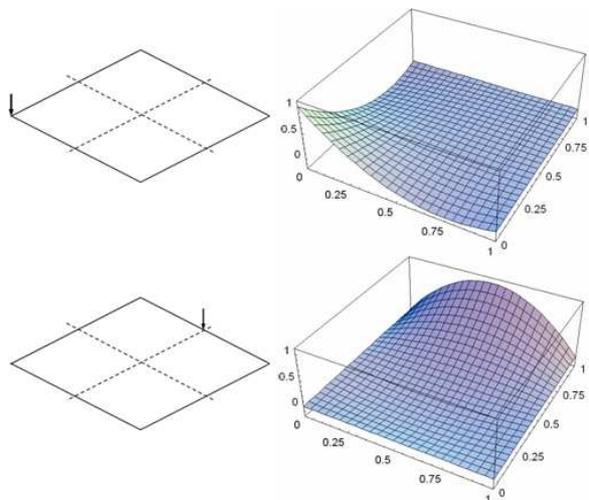


Fig. 3. Two examples for Lagrange polynomials of order two. The right pictures represent the heat flow distribution over the surface for the ports one and eight

two examples for the Lagrange polynomials. Assuming the grid indicates the mesh (in right pictures), the shape of each Lagrange polynomial shows the heat flow distribution on the surface for two different load steps. This procedure simplifies the network model representing the convection significantly, because the relationships between the nodes are defined in ANSYS' load step files.

III. IMPLEMENTATION IN NETWORK SIMULATOR

Using the high-level analog behavioral description language Verilog-A, modules are generated, which can be implemented in many network simulators.

A. Verilog-A Module for Reduced Models

A thermal network described by Eq. (3) can be written as:

Verilog-A module

```
//Verilog-A code for a network module
#include "disciplines.vams"

module mod_name(yio);

//define external nodes
inout [1:n] yio; thermal [1:n] yio;

//define internal nodes
thermal [1:m - n] yint;

analog
begin
  "include "./model.h"
end

endmodule
```

The ports *yio* describe the external IO-ports. Internal nodes of the network are represented by *yint*. Finally, the included header file *model.h* defines the network.

model.h

```
Pwr(yio[1])<+h1,1*ddt(Temp(yio[1]));
Pwr(yio[1])<+h1,2*ddt(Temp(yio[2]));
...
Pwr(yio[1])<+h1,n+1*ddt(Temp(yint[1]));
Pwr(yio[1])<+h1,n+2*ddt(Temp(yint[2]));
...
Pwr(yio[1])<+k1,1*Temp(yio[1]);
Pwr(yio[1])<+k1,2*Temp(yio[2]);
...
Pwr(yio[2])<+h2,1*ddt(Temp(yio[1]));
Pwr(yio[2])<+h2,2*ddt(Temp(yio[2]));
...
```

where $h_{i,j}$ and $k_{i,j}$ are the elements of the matrices *H* and *K*, respectively. Due to the complexity of the network, the above listing shows only some exemplary terms.

B. Verilog-A Module for Convection

The module for convection described by the Lagrange polynomials can be written as:

Verilog-A module

```
//Verilog-A: model for convection
// with Lagrange polynomials

#include "disciplines.vams"

module mod_conv(to_area);

//define external nodes
inout [1:s] to_area;
thermal [1:s] to_area;

//parameter list
parameter real h=1 exclude 0; // film coefficient
```

```
parameter real Tamb=1; // ambient temperature

analog
begin
  Pwr(to_area[1])<+ h*(Temp(to_area[1])-Tamb);
  Pwr(to_area[2])<+ h*(Temp(to_area[2])-Tamb);
  ...
  Pwr(to_area[s])<+ h*(Temp(to_area[s])-Tamb);
end

endmodule
```

The dimension of *s* must be set depending on the order of Lagrange polynomials (e.g. 9 for order two, 16 for order three, etc.).

C. Main Circuitry File

Now, both Verilog-A modules can be implemented into a SPICE circuitry for instance using:

SPICE circuitry

```
//SPICE code for a circuitry with an
//included Verilog-A modules

.verilog "./mod_board.va"
.verilog "./mod_conv.va"

aboard cv1 ... cv9 ld1 ... ld6 mod_board
aconv cv1 ... cv9 mod_conv h=film Tamb=Tamb
...
```

The file *mod_board.va* represents the Verilog-A module of a printed circuit board (PCB). The nine *cv_i* ports define the connection between the board and the convection model. The remaining ports *ld_i* in the board module represent the connection to a package. File *mod_conv.va* represents the Verilog-A module for the convection with polynomials of order two. Defining the convection as *aconv* now the correct values for the parameters *h* and *Tamb* must be set.

IV. APPLICATION

To demonstrate the entire coupling procedure we chose a package with 28 leads and two different PCBs. The model of the package can be seen in Fig. 4. The PCBs are

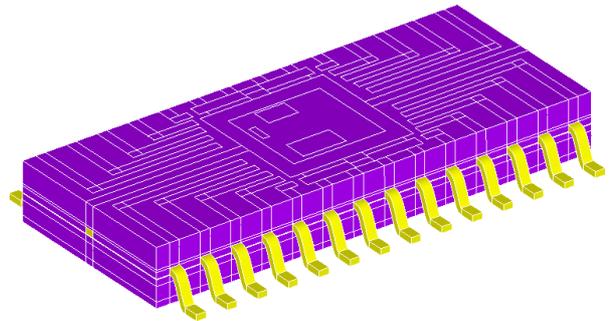


Fig. 4. FE-model of a semiconductor package with three heat sources

JEDEC board 2s2p with two inner Cu layers



JEDEC board 1s with no inner Cu layers

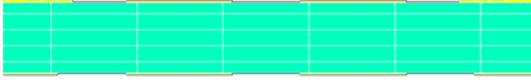


Fig. 5. Board models: 1s JEDEC with only upper copper layer and 2s2p JEDEC with inner copper layers

two JEDEC boards with different copper layer designs. A cross section is shown in Fig. 5. The 1s board has only one signal layer on top. The 2s2p board has two inner and a bottom signal copper layer, additionally.

The models are boundary condition independent, since these conditions are modeled separately. Convection can be described using the representation in Section III-B. In case of a constant temperature, a source with constant voltage can be used. To get an idea of the coupling procedure, Fig. 6 shows the interconnections between the models. The

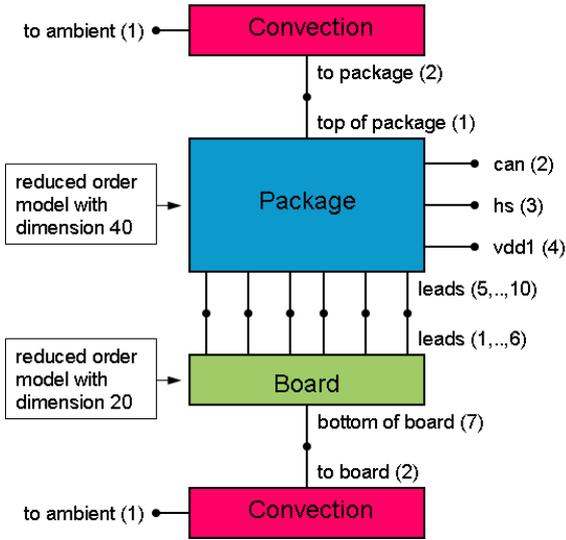


Fig. 6. Model coupling. The numbers in brackets indicate the IO-ports within each model

numbers in brackets indicate the port numbers. Because of simplicity the convection model is represented by a two port model providing only one connection to a surface. Another simplification is the treatment of leads. They are collected into six groups.

V. RESULTS

To verify the network model two simulations with coupled subnetworks has been compared with appropriate ANSYS simulations. The simulations with ANSYS has been made using the full model including package, boards and convection as boundary conditions. For the

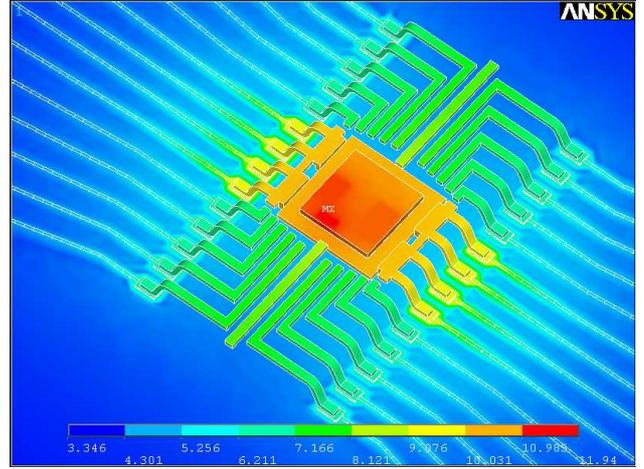


Fig. 7. Steady state results of the full model including PCB, package and convection. Mold compound is removed to see the heat sources on top surface of the die

simulations with network simulator ANSYS models of each subsystem has been reduced: one model for package and two different models for the boards. Finally, they have been coupled in the SPICE simulator. In Fig. 7 temperature distribution for the package on the 2s2p board can be seen for steady state. The simulation in ANSYS was performed using the full model. Here, mold compound is removed for a better view on the temperature distribution on the die and lead frame. The six lead groups can be identified here also very easy. In order to get the same conditions as for the coupled model simulations in SPICE all nodes representing the interconnecting IO-ports has been modified by the use of the CP-command. E.g. this modification can be noticed in Fig. 7 by the homogeneous temperatures within the grouped leads.

Table I shows the temperature on three different positions on the die as a comparison between the full ANSYS model and the coupled network model. As can be seen, the

TABLE I
COMPARISON BETWEEN ANSYS AND A COUPLED NETWORK

Board	JEDEC 2s2p		JEDEC 1s	
Position	ANSYS	SPICE	ANSYS	SPICE
1	11.56 °C	11.72 °C	13.76 °C	13.95 °C
2	11.94 °C	12.09 °C	14.14 °C	14.32 °C
3	11.35 °C	11.51 °C	13.55 °C	13.73 °C

difference stays always under 1.5 %. Also, the board with more copper layers (2s2p) shows smaller temperatures, which is generally always true. Fig. 8 shows transient results at the same three positions calculated using the network simulator. The influence of different boards can be seen very well. Since the package model is the same in both cases the time constants stays untouched, as well. The vertical white line indicates in Fig. 8 the position,

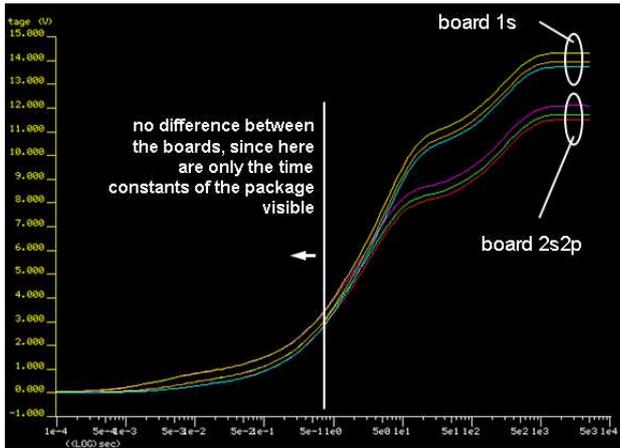


Fig. 8. Transient results of a network simulation with coupled models

where the dynamic response begins to change caused by different boards.

VI. CONCLUSIONS

The paper presents thermal modeling of semiconductor electronics systems using a new compact network model. The model is generated by using model order reduction methods. By generating sub models for the particular elements such as package and the printed circuit board, simulations with coupled models has been performed using an electrical network simulator. The results has been compared with ANSYS simulations using full models and show very small differences. The method provides many advantages such as:

- no geometrical limits
- totally free choice of input functions
- boundary independent models
- very fast calculation time

The remarkable disadvantages of this method are:

- linear material properties
- homogenous potentials at areas defining the IO-ports

Anyhow, keeping the areas small the error caused by the necessary constraint on the IO-ports can be minimized to a negligible value.

REFERENCES

- [1] A. Augustin, A. Kostka, and B. Maj: "Two-dimensional temperature fields in ASICs for multiple heat sources of arbitrary power dissipation derived from conformal mapping theory", *THERMINIC Proceedings*, 2005, pp. 17-24
- [2] N. Rinaldi: "Thermal analysis of solid-state devices and circuits: an analytical approach", *Solid-State Electronics*, vol. 44, 2000, pp. 1789-1798
- [3] ANSYS Inc., <http://www.ansys.com>
- [4] A. C. Antoulas, D. C. Sorensen: "Approximation of large-scale dynamical systems: An overview", *Applied Mathematics & Computer Science* 11, (5) 2001, pp. 1093-1121
- [5] E. B. Rudnyi, J. G. Korvink: "Review: Automatic Model Reduction for Transient Simulation of MEMS-based Devices", *Sensors Update v. 11*, 2002, pp. 3-33
- [6] T. Bechtold, E. B. Rudnyi, and J. G. Korvink: "Automatic generation of compact electro-thermal models for semiconductor devices", *IEICE Transactions on Electronics*, vol. E86C, 2003, pp. 459-465
- [7] Y.-J. Yang, C.-C. Yu: "Extraction of heat-transfer macromodels for MEMS devices", *Micromech. Microeng.*, 14, 2004, pp. 587-596
- [8] A. Augustin, T. Hauck, B. Maj, J. Czernohorsky, E. B. Rudnyi and J. G. Korvink: "Model Reduction for Power Electronics Systems with Multiple Heat Sources", *THERMINIC Proceedings*, 2006, pp. 113-117
- [9] A. Ammous, S. Ghedira, B. Allard, H. Morel, and D. Renault: "Choosing a thermal model for electrothermal simulation of power semiconductor devices", *IEEE Transactions on Power Electronics*, vol. 14, 1999, pp. 300-307
- [10] L. Codecasa, D. D'Amore, and P. Maffezzoni: "Compact modeling of electrical devices for electrothermal analysis", *IEEE Transactions on Circuits and Systems I-Fundamental Theory and Applications*, vol. 50, 2003, pp. 465-476
- [11] H. Vinke and C. J. M. Lasance: "Compact models for accurate thermal characterization of electronic parts", *IEEE Transactions on Components Packaging and Manufacturing Technology Part A*, vol. 20, 1997, pp. 411-419
- [12] C. J. M. Lasance: "Two benchmarks to facilitate the study of compact thermal modeling phenomena", *IEEE Transactions on Components and Packaging Technologies*, vol. 24, 2001, pp. 559-565
- [13] P.J. Heres: "Robust and efficient Krylov subspace methods for model order reduction", *PhD Thesis*, 2005, Eindhoven University of Technology
- [14] L. Codecasa, D. D'Amore, P. Maffezzoni and N. Spennagallo: "A novel approach for generating dynamic compact models of thermal networks having large number of power sources", *Therminic 2005 Proceedings*, 2005, pp. 25-31
- [15] J. M. Dorkel, P. Tounsi, and P. Leturcq: "Three-dimensional thermal modeling based on the two-port network theory for hybrid or monolithic integrated power circuits", *IEEE Transactions on Components Packaging and Manufacturing Technology Part A*, vol. 19, 1996, pp. 501-507
- [16] L. Codecasa, D. D'Amore, and P. Maffezzoni: "An Arnoldi based thermal network reduction method for electro-thermal analysis", *IEEE Transactions on Components and Packaging Technologies*, vol. 26, 2003, pp. 186-192
- [17] T. Bechtold, E. B. Rudnyi and J. G. Korvink: "Error indicators for fully automatic extraction of heat-transfer macromodels for MEMS", *Journal of Micromechanics and Microengineering*, v. 15, No. 3, 2005, pp. 430-440
- [18] <http://www.imtek.uni-freiburg.de/simulation/mor4ansys/>
- [19] R. W. Freund: "Krylov-subspace methods for reduced-order modeling in circuit simulation", *Journal of Computational and Applied Mathematics*, Vol. 123, pp. 395-421, 2000